REMARKS/ARGUMENTS

This Response responds to the Office Action dated February 2, 2009, in which the Examiner rejected claims 1-23 under 35 U.S.C. § 103.

Claim 1 claims a compression encoder, claim 6 claims a compression-encoding method, claim 11 claims a recorder and claim 18 claims a recording method. The compression encoder, compression method, recorder and recording method comprise dividing input first and second digital input signals, having frame rates different from each other into plural macro blocks for each frame. The macro blocks are then rearranged in each frame into groups based on the frame rate and macro block units are created for every group by a shuffling section. The digital image signals for every macro block unit are then compression encoded. The macro blocks of the first digital image signal are rearranged such that an output order of the macro block units of the first digital image signals after compression-encoding is equivalent to the output order of the macro blocks units of the second digital image signal.

By (a) having first and second digital images input with different frame rates, (b) having a shuffling section which rearranges the macro blocks in each frame into groups based on the frame rate and creates macro block units for every group, and (c) having the macro blocks of the first digital image signals rearranged such that an output order of the macro block units of the first digital image signals after compression-encoding is equivalent to the output order of the macro blocks of the second digital image signals as claimed in claims 1, 6, 11 and 18, the claimed invention provides a compression encoder, compression encoder method, recorder and recording method in which the number of decoders necessary for half-speed reproduction of the first image signal can be reduced so that deterioration of resolution can be restricted without

needing an interpolation processing. The prior art does not show, teach or suggest the invention as claimed in claims 1, 6, 11 and 18.

Claim 25 claims a compression encoder, claim 26 claims a compression-encoding method, claim 27 claims a recorder and claim 28 claims a recording method. The compression encoder, compression-encoding method, recorder and recording method include dividing first and second digital image signals into plural macro blocks for each frame. The plural macro blocks in each frame of the second digital image signal are rearranged into groups based on frame rate and macro block units are created for every group. The second digital image signals are rearranged into a layout of macro block units after compression-encoding which is equivalent to that of the first digital image signal. The rearranged plural macro blocks are then compression-encoded.

By (a) having first and second digital images with different frame rates, (b) rearranging the plural macro blocks of the second digital image into groups based on frame rate and creating macro block units for every group and (c) having a layout of macro block units after compression-encoding be equivalent for the first and second digital image signals as claimed in claims 25-28, the claimed invention provides a compression-encoder, compression-encoding method, recorder and recording method which requires no interpolation process when performing a half-speed reproduction so that resolution can be prevented from deteriorating. Furthermore, only one decoder is necessary during reproduction. The prior art does not show, teach or suggest the invention as claimed in claims 25-28.

Claims 1-2, 4, 6-7, 9, 11-14, 16, 18-21, 23 and 25-28 were rejected under 35 U.S.C. § 103 as being unpatentable over *Miller, et al.* (U.S. Patent No. 5,146,324), in view of *Katata, et*

al. (U.S. Patent No. 6,714,591) and further in view of *Elmaliach, et al.* (U.S. Patent No. 5,847,760).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. § 103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicants respectfully request the Examiner withdraws the rejection to the claims and allows the claims to issue.

Miller, et al. appears to disclose in FIG. 1 an input digital video signal 1 to be compressed, and transmitted over a data channel, or recorded and played back on a recording device, and then uncompressed and output as digital signal 2 (Col. 5, lines 1-5).

Thus, *Miller, et al.* merely discloses an input signal 1 and an output signal 2. Nothing in *Miller, et al.* shows, teaches or suggests (a) input first and second digital image signals as claimed in claims 1, 6, 11, and 18, or (b) compressing first and second digital image signals as claimed in claims 1, 6, 11, 18 and 25-28. Rather, *Miller, et al.* merely discloses a single input signal 1 which is compressed.

Additionally, *Miller, et al.* merely discloses block shuffler 10 accepts luminance data and chrominance data, partitions it into predetermined blocks of data and rearranges the data blocks within each field of video. (Col. 5, lines 11-14).

Thus, *Miller, et al.* merely discloses rearranging the data blocks within the single input signal 1. Nothing in *Miller, et al.* shows, teaches or suggests rearranging the macro blocks of a first (second) digital image signal such that an output order of the macro block units of the digital image signal is equivalent to the output order of the macro block units of a second (first) digital image signal as claimed in claims 1, 6, 11, 18 and 25-28. Applicants respectfully request the Examiner point out where in FIG. 1 and Col. 5, lines 11-20 the block shuffler 10 rearranges the

macro blocks of the first (second) digital image signal equivalent to the output order of the macro block units of the second (first) digital image signal. Applicants respectfully point out that *Miller, et al.* only discloses a single input signal 1. Therefore, *Miller, et al.* cannot rearrange the input digital video signal 1 according to another input signal. Rather, *Miller, et al.* only discloses the block shuffler 10 partitioning the data from the input digital video signal 1 into blocks of data which are rearranged.

Furthermore, *Miller, et al.* merely discloses that block shuffler 10 rearranges the data into a time order corresponding to the physical blocks in the image and further scrambles the data by selecting blocks in an order other than the original sequence of blocks in the image (Col. 6, line 68 – Col. 7, line 4).

Thus, *Miller, et al.* merely discloses arranging data in a time order. Nothing in *Miller, et al.* shows, teaches or suggests rearranging plural macro blocks in each frame into groups based upon frame rate as claimed in claims 1, 6, 11, 18 and 25-28. Rather, *Miller, et al.* only discloses arranging data into a time order.

Finally, since *Miller, et al.* only discloses input signal 1 and output signal 2, nothing in *Miller, et al.* shows, teaches or suggest first and second digital image signals having frame rate different from each other as claimed in claims 1, 6, 11, 18 and 25-28. Rather, *Miller, et al.* merely discloses a single input signal 1 and an output signal 2.

Katata, et al. appears to disclose a video coding device having a first coding mode in which an entire image is encoded, and a second coding mode in which only a partial area (e.g. a speaking person area or a facial portion) in the image is encoded (Col. 4, lines 52-56). A coding device may be enabled to encode, in case of encoding of a part image containing only a speaking person region, mouth area and other area at different frame rates (Col. 9, lines 34-40).

Thus, *Katata, et al.* discloses a single input image data encoded at different frame rates based on a partial area. In other words, the encoding in *Katata, et al.* is done at different frame rates. *Katata, et al.* does not disclose (a) input first and second digital images and (b) that the first and second digital image signals have different frame rates from each other as claimed in claims 1, 6, 11, 18 and 25-28. Rather, *Katata, et al.* only discloses that the encoding of the (single) image is encoded at different frame rates.

Furthermore, *Katata, et al.* only discloses it is possible to encode a partial area of a part image at a different frame rate than the other area (Col. 11, lines 7-10).

Thus, *Katata, et al.* only discloses encoding part of an image at a different frame rate. Nothing in *Katata, et al.* shows, teaches or suggests rearranging macro blocks into groups based upon frame rate as claimed in claims 1, 6, 11, 18, and 25-28. Rather, *Katata, et al.* only discloses encoding a partial region at a different frame rate.

Finally, since *Katata, et al.* only discloses encoding part of a single input image at a different frame rate, nothing in *Katata, et al.* shows, teaches or suggests an output order of macro block units of a first (second) digital image signal is equivalent to the output order as macro block units of a second (first) digital image signal as claimed in claims 1, 6, 11, 18, and 25-28. Rather, *Katata, et al.* only discloses a single input image signal which may be encoded at different frame rates.

Elmaliach, et al. appears to disclose a method and system providing a plurality of compressed presentations of each frame of an original video signal, each presentation provided according to a different bit rate. The transmitting system selects from the compressed presentations a presentation which is most suitable for the bit-rate currently available over the transmission line (Abstract).

Thus, *Elmaliach, et al.* merely discloses a single original video signal which is compressed a plurality of ways based on bit-rate. Nothing in *Elmaliach, et al.* shows, teaches or suggests (a) first and second digital image signals and (b) different frame rates for each of the first and second digital image signals as claimed in claims 1, 6, 11, 18 and 25-28. Rather, *Elmaliach, et al.* only discloses a single original video signal which is compressed a plurality of ways.

Additionally, *Elmaliach, et al.* merely discloses encoder 4 processes a frame set and converts it into three MPEG frame sets 10, 20 and 30. The encoder 4 provides frame-set 10 according to the maximal bit-rate which is available. The encoder 4 provides frame-set 20 according to half the maximal bit-rate which is available. The encoder provides frame-set 30 according to a quarter of the maximal bit-rate which is available (Col. 3, lines 49-65). The encoder 4 includes a compression controller 3 and three encoding processors 5, 7, and 9 (Col. 4, lines 15-17). The encoding processor 5 generates frame-set 10, encoding processor 7 generates frame-set 20, and encoding processor 9 generates frame-set 30 (Col. 4, lines 25 – 28).

Thus, *Elmaliach, et al.* only discloses encoding the original video signals into three frame sets 10, 20 and 30. Nothing in *Elmaliach, et al.* shows, teaches or suggests rearranging macro blocks in each frame into groups based on frame rate as claimed in claims 1, 6, 11, 18 and 25-28. Rather, *Elmaliach, et al.* only discloses encoding the original video signal into three frame sets.

Finally, *Elmaliach, et al.* merely discloses a controller 40 selects GOPs from one of the frame sets 10, 20 and 30 according to the bandwidth/bit-rate available (Col. 5, lines 11-24, Col. 6, lines 21-63). Nothing in *Elmaliach, et al.* shows, teaches or suggests rearranging macro blocks of a first (second) digital image signal such that the output order of the macro block units

of the digital image signal after compression-encoding is equivalent to the output order of the macro block units of a second (first) digital image signal as claimed in claims 1, 6, 11, 18 and 25-28. Rather, *Elmaliach, et al.* only discloses selecting one of the frame sets for transmission based upon the bit-rate currently available over the transmission line.

A combination of *Miller, et al.*, *Katata, et al.* And *Elmaliach, et al.* would merely suggest to input a single digital video signal into a block shuffler 10 and taught by *Miller, et al.*, to encode different parts of the image at different frame rates as taught by *Katata, et al.*, and to provide at least three different frame sets according to different bit rates so that a transmitter can transmit the proper bit rate based upon the bit-rate of the transmission line as taught by *Elmaliach, et al.* Thus, nothing in the combination of the references shows, teaches or suggests (a) input first and second digital image signals, (b) compressing first and second digital image signals having different frame rates, (c) rearranging macro blocks into groups based on frame rate, and (d) rearranging macro blocks of a first (second) digital image signal such that the output order thereof is equivalent of an output order of a second (first) digital image signal as claimed in claims 1, 6, 11, 18 and 25-28. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claims 1, 6, 11, 18, and 25-28 under 35 U.S.C. § 103.

Claims 2, 4, 7, 9, 12-14, 16, 19-21 and 23 depend from claims 1, 6, 11 and 18 and recite additional features. Applicants respectfully submit that claims 2, 4, 7, 9, 12-14, 16, 19-21 and 23 would not have been obvious within the meaning of 35 U.S.C. § 103 over *Miller, et al., Katata, et al.* and *Elmaliach, et al.* at least for the reasons as set forth above. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claims 2, 4, 7, 9, 12-14 16, 19-21 and 23 under 35 U.S.C. § 103.

Claims 3, 8, 15 and 22 were rejected under 35 U.S.C. § 103 as being unpatentable over *Miller, et al.*, *Katata, et al.*, and *Elmaliach, et al.* in view of *Chen, et al.* (U.S. Publication No. 2003/0138051). Claims 5, 10, 17 and 24 were rejected under 35 U.S.C. § 103 as being unpatentable over *Miller, et al.*, *Katata, et al.* and *Elmaliach, et al.* in view of *Porter, et al.* (U.S. Patent No. 7,227,900).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. § 103. The claims have been reviewed in light of the Office Action and for reasons which will be set forth below, Applicants respectfully request the Examiner withdraws the rejection to the claims and allows the claims to issue.

As discussed above, since nothing in *Miller, et al.*, *Katata, et al.* and *Elmaliach, et al.* show, teach or suggest the primary features as claimed in claims 1, 6, 11 and 18, Applicants respectfully submit that the combination of the primary references with the secondary reference to *Chen, et al.* or *Porter, et al.* will not overcome the deficiencies of the primary references. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claims 3, 5, 8, 10, 15, 17, 22 and 24 under 35 U.S.C. § 103.

The prior art of record, which is not relied upon, is acknowledged. The references taken singularly or in combination do not anticipate or make obvious the claimed invention.

Thus, it now appears that the application is in condition for a reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested. Should the Examiner find that the application is not now in condition for allowance, Applicants respectfully request the Examiner enters this amendment for purposes of appeal.

CONCLUSION

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to Deposit Account No. 50-0320.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 50-0320.

Respectfully submitted,

FROMMER LAWRENCE & HAUG LLP
Attorneys for Applicants

Date: April 2, 2009

By: _____
Ellen Marcie Emas
Reg. No. 32,131
Tel. (202) 292-1530